Semiconductor Process Synthesis: Virtual Reactor and Recipe Synthesis Frameworks for Rapid Equipment and Process Development

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Project Summary

Fabrication equipment design/improvement and unit process recipe development are among the major contributors to the overall cost and cycle time of semiconductor technology development. Our work has focused on establishing and demonstrating the foundation for a generic and systematic concurrent equipment and process engineering methodology for rapid equipment design, rapid unit process characterization and recipe synthesis. This methodology has been demonstrated via the development of a virtual reactor framework for single-wafer thermal processing (RTP, RTCVD, MOCVD) equipment. We have undertaken a relatively small, focused aspect of a much larger process synthesis integrated design environment in which all of the top-down product-level requirements and bottom-up equipment constraints as well as the significant unit process interactions must be characterized, modeled, and represented as physical design rules at various levels of model building and process synthesis. The task of unit process synthesis has been accomplished based on a combination of simulated runs in a virtual factory (consisting of virtual reactors along with models for wafer state and equipment state changes) and a reduced number of silicon runs (resulting from the use of smart-flow test structures and intelligent recipe synthesis methodologies). The virtual reactor has been developed by using advanced control software design tools to create an integrated environment for Equipment CAD, Intelligent Design of Experiments, Process Control, Sensor Fusion, and Recipe Synthesis. This system has been demonstrated for the development of an RTP temperature control system. Although our study was concerned with one class of fabrication processes, the demonstrated methodologies are applicable to a wide range of unit processes required for most semiconductor process flows. This virtual reactor development project is consistent with the process synthesis ideas established to date at leading semiconductor companies and universities.

1 Introduction

Continuous scaling and development of advanced high-performance semiconductor technologies is essential for numerous applications including computer systems, consumer electronics, and telecommunication systems. The performance, development cost, and manufacturing cost parameters associated with a newly developed semiconductor technology directly influence the performance and cost of the resulting information technology products.

The current practice of semiconductor technology development is based on a complex combination of numerous iterative tasks based on two sets of boundary conditions. The high-level boundary conditions are a set of system-level product performance, reliability, and cost requirements. The low-level boundary conditions are essentially the device fabrication capabilities as determined by the available processing equipment set. These "top-down" requirements and "bottom-up" capabilities define the domain and constraints for semiconductor technology development. The need for numerous experimental iterations in conjunction with many pilot experiments as well as short-flow and full-flow silicon runs arises because of the lack of model-based systematic methodologies for unit process specifications, layout design rule specifications, development and integration of unit processes, as well as integration of the overall process flow. The current practice of semiconductor technology development depends on many time consuming sequential and empirical engineering steps with minimal concurrent process engineering.

In general, the semiconductor technology development process can be divided into a number of tasks including: (1) end-product definition, (2) product mix definition, (3) semiconductor technology definition, (4) test-structure design, (5) transistor device and/or memory cell design, (6) initial process flow definition, (7) initial layout design rules, (8) unit process requirement documents (PRDs), (9) unit process development, (10) process flow integration, (11) final layout design rules, (12) device parameter extraction, and (13) productization and manufacturing ramp-up. The current practice has many interdependent and sequential process engineering steps at all levels from the unit process development to the final process integration. The process characterization and development tasks are not efficiently divided between the unit process development activity and the overall process integration activity. Most of the unit process PRD parameters deal with the unit process and wafer state parameters at a localized level without any consideration of the short- and long-range unit process interactions. The PRD parameter sets and wafer state definitions (i.e., incoming and outgoing wafer states) are rather empirical and do not include standardized parameter sets to deal with the flow-level unit process interactions. As a result, the individual unit processes are mostly developed and verified based on rather simplistic methodologies using pilot wafers and short-flow silicon experiments. Once the PRD specifications are met for a given unit process, that process is considered to be ready for integration into the process flow. There are, however, additional integration-level requirements for each unit process. For instance, usually a silicide anneal unit process PRD includes specifications for the blanket silicide sheet resistance values (e.g., mean, uniformity and repeatability) for the silicide layers formed on n+ Si, p+ Si, and doped polysilicon gates. In the conventional method of unit process development, the unit process is claimed to be ready once these requirements are met on blanket doped wafers with specified doping levels. The unit process development task usually ignores the unit process integration requirements which are usually more stringent due to the unit process and wafer state interactions. For instance, a silicide anneal process must meet additional requirements in the process flow. These requirements include low junction leakage (interactions with source/drain junction anneal), negligible transistor series resistance degradation due to junction dopant loss (again, interactions with source/drain junction anneal), and acceptable sheet resistance for narrow lines (narrow silicided gates show higher sheet resistance than blanket layers). A given unit process may easily meet the standard PRD parameter specifications but fail to meet the process flow requirements. This places a significant burden on the process integration activity to fully verify and retune all of the individual unit processes. This usually requires multiple iterations until all of the unit processes are successfully integrated into the process flow.

Figures 1 and 2 illustrate a generic method of the current practice for development of new fabrication equipment and unit process recipes. In most cases, the vendor-driven equipment development cycle stops

prior to the indicated vendor/user process co-development and equipment improvement program activity. All of the subsequent equipment and process characterizations as well as the final unit process development, characterization, and integration are performed by the user after a piece of equipment is delivered to the user's fab. However, this trend in the equipment development programs is changing. For instance, some equipment vendors are now using advanced equipment CAD to optimize the initial equipment design (as shown in Figure 1). Moreover, there are increased cases of vendor/user partnerships during the equipment development cycle prior to its delivery to the user. These procedures will ensure that a new piece of equipment will meet the user's process requirements in a timely manner once it has been delivered. Figure 2 illustrates a generic current methodology for development, characterization, and integration of unit processes into a process flow. This figure shows various required tasks for complete unit process development and integration. These tasks are currently divided between the unit process development and process integration activities. In some cases, such as the development of a derivative of an existing unit process, some of the subtasks shown in Figure 2 are eliminated. In the current practice, the unit process development cycle is considered complete when the full PRD parameters are met. The subsequent unit process module-level and flow-level integration activities are performed as part of the process integration cycle, resulting in numerous iterative experiments affecting the unit process parameters and the PRDs.

In this final Phase I report, we describe and demonstrate a unit process synthesis methodology for a specific, focused application based on systematic model-based concurrent process engineering. The impact of this unit process synthesis strategy on the technology development and cycle time reduction will be quite significant. For example, our approach dictates a methodology for concurrent fabrication equipment design and unit process characterization based on a virtual reactor framework. The equipment design activity must be based on well-defined, projected unit process requirements for a range of technology nodes and generations. A new fabrication equipment must be designed to provide a wide process window and excellent process control for enhanced process yield, equipment reliability, and equipment capability to handle scaled unit processes. The unit process specifications must also comprehend all of the flow-level unit process and wafer state interactions. Equipment CAD based on physical, mechanical, chemical and cost-of-ownership models will be used in conjunction with models for sensors and process control algorithms in order to design the equipment (or to improve the performance/reliability of an existing fabrication equipment) for wide process windows and maximum process/tool scalability for reduced processing cost per wafer. Whenever a new fabrication equipment is needed, the equipment development program must be performed in parallel with unit process characterization and modeling. A new fabrication equipment should include complete models of the equipment and process over a wide range of operating conditions within a virtual reactor framework to enable rapid unit process recipe synthesis. These models are calibrated and used during the process development, process characterization and recipe synthesis and also as virtual reactor modules within the virtual wafer factory. Moreover, these embedded models can be used to design optimum process controllers and to establish the optimum sensor fusion design rules for specific applications.

2 Process Synthesis Framework

Our process synthesis approach has been constructed to eliminate the highly iterative and empirical nature of the semiconductor fabrication equipment design and process development operations. An overall, fully integrated process synthesis medium that will interface with the IC manufacturing environment is illustrated in Figure 3 and follows the process synthesis approach at Texas Instruments (while at TI, Dr. Mehrdad Moslehi, a principal investigator on this program, managed the process synthesis group). The process synthesis environment consists of a Unit Process and Module Synthesis System, a Flow Synthesis System and a Process Module Library. The manufacturing facility consists of a real factory, simulated factory and an associated factory CIM system. The total process synthesis capability is linked by an Integrated Design Environment (IDE) that includes a shared information infrastructure. The IDE will integrate all of the process synthesis components, the CIM System, and CAD tools. The IDE assists the process engineer in conducting process synthesis tasks, using a combination of simulated and real experiments following systematic methodologies. This proposed approach offers a scalable and flexible design environment which can be applied to synthesis of many generations of scaled and derivative semiconductor technologies.

In this Phase I program, we developed modules and strategy for a Virtual Reactor (VR) Framework and a Recipe Synthesizer (RS) Framework for single-wafer thermal processing equipment. These frameworks constitute components of the Unit Process & Module Synthesis System. This system enables equipment and process engineers to quickly design fabrication equipment and synthesize unit processes and modules in response to requirements generated by the flow synthesis framework. The first step in this methodology is to identify the unit processes associated with the modules. Integration design rules, equipment constraints, cost, performance, reliability and yield requirements will then be used to establish the equipment and unit process specifications. Unit processes and associated modules will be synthesized based on these specifications and verified through simulated and actual silicon runs. The design rules and process models will be established based upon the results from these runs. Finally, synthesized process modules will be incorporated into the module library.

The VR framework of the Unit Process & Module Synthesis System provides a seamless hierarchical design environment that includes tools for equipment and unit process design and associated process equipment interfaces. The VR framework includes models of the fabrication reactors in the factory (for various classes of unit processes) and their sensors. It also provides flexible sensor fusion and controller synthesis tools to develop optimum process control and diagnosis strategies for technology synthesis and manufacturing. The VR framework performs simulated fabrication experiments in conjunction with the simulated factory environment in response to recipe synthesizer (RS) requests. The RS framework enables verification and validation of the process sequence via experimental runs in the simulated factory, and whenever necessary in the real factory. The synthesized process sequence is stored in a reusable multilevel module library.

Our objective for this Phase I program is to develop the framework for the critical development of a virtual reactor. This framework can be used as part of an overall process synthesis structure described above. To achieve the development of the virtual reactor, our efforts have been directed in the following areas:

- **Equipment CAD:** Develop a focused approach to systematize equipment development through the use of models that relate equipment parameters and settings to the process boundary conditions (i.e. treatments) at the surface of the wafer.

- **Recipe Synthesis:** Formalize procedures to automatically and rapidly converge to an optimum unit process recipe with minimal experimental iterations for characterizing and verifying the process.

- **Sensors and Process Control:** Conceive a strategy to fully utilize and/or optimize integrated sensors (sensor fusion) and process control strategies within the virtual reactor framework

Although this study was restricted to the single-wafer thermal processing (RTP, RTCVD, and MOCVD) equipment, we envisage that the methodologies will be applicable to several other semiconductor manufacturing processes. Moreover, the structures developed in this Phase I program are consistent with the larger process synthesis architecture that characterizes the system in a hierarchical process module representation. This approach will ultimately allow the combination of real-time data from the factory CIM system with process models in a simulated factory to allow accurate concurrent development of all parts of the semiconductor technology. This will reduce the technology development cost and cycle time.

In this section, frameworks are described for a virtual reactor for single-wafer thermal processing (RTP, RTCVD, MOCVD) applications. We developed the flexible virtual reactor framework such that it can be embedded within the fabrication equipment, software environment and then the overall integrated process synthesis architecture described above. This architecture is presented in more detail in Figure 4 in which we are concerned with the most important aspects of the virtual reactors and recipe synthesizer tasks for applications in thermal processing fabrication equipment design and integration. Although the Phase I work is focused on a single class of processes and manufacturing equipment, we believe that the techniques are generic methodologies and will be applicable to most semiconductor manufacturing processes and associated fabrication equipment.

2.1 Equipment CAD

We have developed and demonstrated a software/hardware approach to integrate modeling tools for single-wafer rapid thermal processing (RTP) systems into an Equipment CAD framework. It is first necessary to describe the overall concept of the Equipment CAD tool to discuss the integration.

Equipment development and improvement constitutes a large portion of the overall time and cost to develop new unit processes. The rapid increase in processing complexity, the increase in wafer diameter, and more stringent processing specifications are decreasing the useful lifetime of processing equipment. Iterating on equipment designs is time consuming and expensive. A systematization of equipment development and improvement using equipment CAD affords several benefits for accelerating equipment improvement and new equipment development. Equipment CAD (EqCAD) refers to approaches for systematizing equipment development or improvement through the use of models that relate equipment parameters and settings to the process boundary conditions at the surface of the wafer. These models typically lack the detail of the unit process models that are used for microscopic analysis of the phenomenon, but are suitable for addressing issues of processing rate and macroscopic uniformity. Often, these two process parameters are the most significant during the early stages of equipment development. However, other parameters that also critically depend on the equipment design may have to be considered (e.g., plasma parameters for plasma processes, species directionality for sputter deposition, and temperature ramp rates for RTP equipment).

Equipment CAD can be used in a variety of ways during all phases of equipment development and improvement. In the area of improvement and optimization, equipment CAD can be used to evaluate equipment modifications for enhancing all of the process performance parameters that depend on the equipment design, or for establishing new unit processes for a scaled technology node or a derivative technology. Equipment CAD reduces iterations of alternative designs that are actually built and tested. Designs of new equipment must ensure that the widest possible process domains have been achieved for maximum equipment lifetime over multiple technology nodes. The concept of a virtual reactor that is based on an equipment model is especially powerful. Such virtual reactors can be used for simulating equipment, identifying processing domains, defining the initial process, and developing and testing control algorithms and controllers. The EqCAD models can be used to generate the response functions required for setting up a controller, or they can serve at the heart of a model-based control approach. This can also be used for determining the minimum critical sensor set and sensor fusion strategies required for enabling advanced process control/diagnostics. Use of EqCAD will also promote standardization, of both hardware and software as well as in situ sensors. Equipment CAD must be an integral part of process synthesis if the goal of shortening development times and reducing non-recurring engineering costs is to be realized.

As will be exemplified by our proposed application, the main input variables to the EqCAD models are reactor parameters (e.g., reactor geometry, chamber materials, gas distribution and exhaust, and lamp design) and equipment settings (e.g., pressure, gas flow rates, gas composition, temperature, and power). The outputs of the models describe the environment at the surface of the wafer (i.e., treatments). These models are usually physically based since the ability to predict trends as a function of reactor parameters and equipment settings is often more important than numerically accurate results. In these respects, EqCAD models differ from process models which normally do not include reactor parameters as input variables. However, some EqCAD models such as those for furnaces and RTP equipment can easily be extended to process models by instantiating the model for a pre-defined reactor parameter set and concatenating it with a model that relates the wafer treatments to changes in wafer state. EqCAD models are fairly mature (i.e., predict most first-order effects with adequate accuracy, are calibrated and are verified) for most classes of semiconductor fabrication equipment. Process models must be integrated with the EqCAD models fairly early in the design cycle so that the impact of the design on all parameters of interest for the particular process can be studied. The two should, however, remain distinct to allow for the concept of an equipment driver. The equipment driver will link the equipment settings to the wafer treatment for a particular piece of equipment, while the process model will link the outgoing wafer state to the wafer treatment and the

incoming wafer state. In this manner, the process model will be independent of the equipment model and can be used with a variety of equipment drivers.

Despite the maturity of the models for most processing tools, EqCAD is only slowly gaining acceptance. Part of the reluctance can be attributed to poor user interfaces, and the lack of model realism. An EqCAD framework that allows the user to set up the reactor configuration and specify the input and output variables without worrying about the details of the solution technique is essential. The framework should provide an intuitive graphical interface, automate the simulation sequence, incorporate data libraries and intelligence, and use standard computational engines whenever possible. The framework should be configurable for the various applications of EqCAD (e.g., equipment type selection, simulation, process domain identification, process characterization, controller development, equipment driver development, and testing and validation). A proposed framework is graphically described in Figure 5. It highlights the major blocks that need to be a part of the framework. In the inputs section, the user should be able to specify all of the equipment settings, the reactor geometry, and the desired outputs. Transfer interfaces will allow this framework to be linked with other modules. Draw tools and pre-defined reactor geometry's should provide flexibility in specifying the reactor design. The interface should also permit the user to specify material properties and provide a library of choices. Many of the EqCAD models can only deal with simplified geometry's, and the framework should include simplification tools that rely on rules and heuristics to simplify the user specified reactor geometry to a final geometry that is modeled. The model itself should include blocks for grid generation, selection of the computational engine, solution control, and data libraries (i.e., information on material properties, chemical kinetics, initial guesses, prior solutions, etc.) A model setup and validation block is essential so that the system can make intelligent choices and checks on each of the other blocks on the basis of rules and heuristics. This block will also specify and interpret experimental data required for verification and calibration. The output section will include blocks for the display and manipulation of output data.

The first step in the use of equipment CAD within the equipment development cycle is first to select the type of equipment based on the treatments that are to be achieved at the wafer, the type of technology, the desired throughput, cost-of-ownership and other considerations. The reactor configuration is then defined for the specific equipment type, and the performance of the equipment is simulated. After the first pass design is complete, a process model can be incorporated, and an equipment prototype can be built and tested. Experiments on the prototype are used to calibrate and validate the model. The simulations and prototype testing are iterated until a satisfactory process is achieved. Then the EqCAD framework can be exercised for process domain determination, process characterization, and development of the process controller, sensor fusion and equipment driver. Complete deployment of EqCAD for the discussed applications will yield a significant savings in time and effort involved in equipment development.

We have utilized the EqCAD framework discussed above and developed a virtual reactor environment for single-wafer thermal (RTP, RTCVD, MOCVD) processing equipment. Our approach has utilized a graphical programming environment to represent the unit process and systems operations. Rapid prototyping of alternative design strategies can be quickly evaluated by utilizing this strategy. Examples and discussion of our approach are presented later in this report.

2.2 Recipe Synthesis

We have developed the methodology and software for our thermal processing process synthesis application to enable the model-based recipe synthesis objectives. One of the key elements required of process synthesis is the ability to automatically and rapidly converge to an optimum unit process recipe with minimal experimental iterations for characterizing and verifying the fabrication equipment and its associated unit process. The need to automate and reduce experimentation cannot be over emphasized due to the fact that silicon runs constitute the majority of the cost and time taken for devising a new process flow or a new technology derivative. Thus, a major component of unit process synthesis is recipe synthesis and its place in the process development cycle is illustrated in Figure 6. The input to recipe synthesis would include well defined process specifications and acceptable tolerances, while the output would be a robust,

reliable processing sequence and its associated process parameter trajectories. This process sequence would include the standard active steps as well as complementary steps (e.g., initiation, passivation, stabilization, and pump down, in situ chamber clean, etc.)

An important aspect of a process synthesis strategy will be to define a new methodology to generate a unit process recipe (i.e., recipe synthesis). Before such a methodology is discussed, however, a framework for process synthesis needs to be defined. Figure 7 illustrates an example of one such framework.

At the top of the recipe synthesis framework is the *Process Requirement Document generator (PRD)* which receives input from the flow synthesizer (shown in the flow synthesis framework) about which process needs to be synthesized and its associated specifications and tolerances. The core elements that are part of the entire process synthesis framework are the representations for process, wafer and equipment states. The *Semiconductor Process Representation (SPR)* provides information about the state of a process or a family of similar processes. The information it contains can range widely including physical models, comparisons between similar processes, particular advantages and disadvantages, and characteristic trends. The *SPR* is tightly coupled with *TCAD* tools to facilitate simulations using simulators such as SUPREM, SPEEDIE, PISCES, etc. The *Semiconductor Wafer Representation (SWR)* would be responsible for handling all the details of state transformations a wafer goes through during the course of synthesizing the fabrication processes. It would be linked to a *Sensor Data Bank (SDB)* where all the *in situ* and *ex situ* sensor data are catalogued and stored. Information about the capabilities and condition of any equipment can be obtained from the *Semiconductor Equipment Representation (SEQR).* The *SEQR* is coupled to *Equipment CAD (EqCAD)* tools so that the equipment's behavior can be simulated for various equipment settings.

Two more elements that a play a role in recipe synthesis are the *Process Development Rule Knowledge Base (KB)* and the *Intelligent Designer of Experiments (IDOE).* The *KB* consists of design rules, derived from past experience, to chart out an intelligent and model-based roadmap for recipe building, experimentation, and characterization. The *IDOE*, with the help of *KB*, looks for ways to reduce the experimentation and iterations in process characterization. Finally, the *Recipe Synthesizer* outputs a valid recipe that satisfies all the *PRD* requirements taking its inputs from any one of its five predecessors (as shown in Figure 6) to arrive at a suitable recipe. If the process specifications cannot be met, the *Recipe Synthesizer* generates the necessary information to feed back to the flow synthesis module.

The recipe synthesis requires the development of four subunits: (1) Knowledge Base, (2) Intelligent Design of experiments, (3) Unit Process Recipe Building, and (4) Verification and Validation. These concepts were utilized in developing the framework for recipe synthesis that has led towards a process synthesis strategy for the virtual reactor environment for RTA, RTCVD and MOCVD process applications.

2.3 Sensor Fusion and Process Control

An important aspect of process synthesis involves the integration of sensors and process control strategies within the virtual reactor framework. In this manner, advanced control algorithms can be analyzed efficiently in terms of, for example, the process capability index Cpk of the equipment. Sensor selection, installation, placement and fusion issues can also be assessed. For this Phase I, we developed the integration requirements and specifications of key process and wafer state sensors and sensor fusion rules for RTP, RTCVD, and MOCVD applications within the virtual reactor framework. We will then study the use of such sensors and associated fusion and control algorithms for process synthesis applications.

In a general sense, the block diagram illustrating the different levels of hierarchy for process monitoring and control is shown in Figure 8. The top-level control loop is the determination of process specifications (PRD) and mask geometry for the unit process. This determination is made at the device and circuit design level, and modifications to these specifications will be prompted by final electrical tests on devices and circuits. It is also possible that the compilation of module-level data can prompt changes in the PRD specifications. This constitutes the highest level process control loop, with the initial inputs coming from high level circuit design issues and device performance and reliability requirements.

Recipe generation is at the next level. The recipe generator accepts its initial input in the form of the process specifications and provides a recipe for use in the initial run of the wafers. Recipe generation is determined from short-loop electrical test data (smart flows), material analysis, and compilation of process data. Global optimization techniques are then used to obtain a process recipe which maximizes the predefined figures of merit and stability in the presence of disturbances.

The run-by-run controller gets its initial input from the recipe generator and tunes the recipe between wafer runs based on the data provided by post-process and real-time sensors from the current process (i.e., feedback), as well as pre-process sensors and post-process data from previous processes (i.e., feedforward). Feedback control maintains the process at a local optimum in the presence of disturbances such as drifts and shifts in equipment states as well as starting wafer states. Feedforward control allows the modification to the recipe based on wafer state information taken prior to the processing step.

While the run-by-run controller adjusts the recipe parameters between runs, the real-time controller modifies the equipment settings during a run. The real-time controller accepts inputs from the run-by-run controller and continuously tunes the equipment settings during a process based on measurements provided by in situ sensors. The real-time controller compensates for differences that exist among different runs due to variations in the incoming wafer or equipment states. The differences that can be characterized before the process begins are compensated for by the run-by-run controller using feedforward control. The differences that can only be characterized during the process through the in-situ sensors are compensated for by the real-time controller.

More resources and time have to expended to obtain measurements at higher order control loops. Data analysis also becomes more complicated as the effect of interactions need to be separated from the unit process issues. Higher-order measurements are needed, however, to examine both the short- and long-range interaction effects. To minimize non-recurring engineering cost and process development cycle time, therefore, as many characterizations as possible should be made within low-order control loops with only the critical interaction measurements being performed at the higher order control loops. The concept of verifying quality as soon as it is possible at low levels of synthesis and production is not new. One of the concepts of Total Quality Control (TQC) is that it shifts the responsibility for quality from post-production inspections to the production process itself.

We have utilized this framework to integrate sensors, sensor fusion strategies and process control within the our virtual environment setting.

3 Process Synthesis Implementation and Results

The process synthesis was broken down into the areas of (1) Equipment CAD and virtual reactor, (2) Sensor fusion and intelligent process control, (3) Intelligent design of experiments and recipe synthesis. Examples are presented in this section to demonstrate our approach to these three areas.

3.1 Virtual Reactor Equipment CAD

The strategy shown in Figure 9 was used to develop a process synthesis environment. This approach was developed to link simulation codes with advanced control software for concurrent design of reactor hardware and the associated controller. The modes of operation of this configuration included (1) application of the simulator and control software in a virtual environment, (2) application of control software in a real processing environment or (3) hybrid application of the simulator, control software, and the reactor hardware. Our efforts for Phase I were primarily concerned with formalizing the virtual environment mode of operation for single-wafer rapid thermal processing; The control software environment was developed with capabilities that included graphical model development, advanced control design, numerical simulation capability, and automatic C-code generation. The MATLAB and SIMULINK software toolset available from MathWorks was utilized in our code development and testing.

The process synthesis simulation, sensor fusion, and control development environment is shown in Figure 10. This shows a general approach applicable to both workstation and PC platforms. In fact, the efforts done for the Phase I program were performed primarily using the PC environment. In this approach, data taken from the actual equipment or from a simulator (see Figure 11) was numerically analyzed. A graphical depiction of the systems for the process was then formulated. Upon completion of an appropriate design or configuration, real-time C-code was then automatically generated and compiled for real-time application. A wide variety of problems were undertaken using this strategy including: Equipment CAD to analyze scale-up of the equipment and to evaluate and optimize processing conditions for recipe synthesis; Signal processing for sensor fusion and development of advanced real-time control systems; Intelligent design of experiments to identify an empirical process model by reducing the number of silicon runs.

The modeling architecture shown in Figure 12 was used to simulate the closed-loop control of wafer temperature as well as the real-time growth of oxide and polysilicon films. The modeling architecture begins with a "reference trajectory" which consists of a user-defined set-points for closed-loop control. Any pre-process data that can be used to improve the controller characteristics are represented by the "feedforward" block. The "controller" block represents the multivariable, model-based control algorithm, while the "actuator" represents the process chamber with associated energy sources and gas delivery systems. The "process" represents the interface between the wafer treatment and the final wafer state. Three sources of error, "actuator disturbance", "process disturbance" and "sensor disturbance" are introduced into the appropriate blocks. Each block is a so-called system block which can be comprised of additional modules describing some of the specific features germane to the blocks functionality.

Simulation of the wafer temperature at the center during a controlled RTP thermal cycle is shown in Figure 13. In this simulation run, a nonlinear model relating lamp power to temperature has been used. Multivariable closed-loop control for a five zone axisymmetric RTP lamp has been implemented. Random sensor noise has been introduced into the control loop.

Simulation of oxide growth is presented in Figure 14. For a given closed-loop controlled temperature ramp, the dynamics of oxide growth are obtained through a oxidation model. Thus, an equipment model (equipment CAD) relating power settings to wafer temperature has been integrated with a process model (Deal-Grove oxidation model) relating temperature to oxide thickness to arrive at the full simulation (virtual reactor).

3.2 Sensor Fusion and Process Control

An illustration of the determination of an optimal sensor set to be used for sensor fusion is presented in Figure 15. In order to determine the optimal sensor set for a rapid thermal oxidation process, a model of the interactions of the various components of the process is needed. The left-most column lists the controllable equipment settings. These represent the actual knobs the process engineer can adjust to control the outcome of the process. The second column represents uncontrolled equipment states. These are equipment states that have effects on the process but are to the first order not controllable. The two groups of the equipment settings determine the group of parameters in the intermediary equipment state column, which in turn determine the parameters in the wafer treatment column. The wafer treatments consist of the parameters at the wafer/process ambient interface where the reactions for the oxidation takes place. The changes in the wafer state (effects) is determined by the wafer treatments and pre-process wafer state. Ultimately, the process engineer is interested in obtaining a desired set of changes in wafer state. By charting the interdependencies of the various process parameters, a set of sensors that measures the key parameters can be identified. Parameters with a (1) on the boxes represent parameters which are currently measured. Parameters with a (2) represent a set of strategic advanced sensors. Together, the two groups of sensors comprise the optimal sensor set which are used as inputs to the sensor fusion engine. The selection of the sensors is based on either of two basic criteria. The sensors must be an enabling element of the process. That is, the sensor must allow process control which would enable the equipment to support a particular process. Alternatively, the sensor must reduce the yielded cost of ownership of the tool. That is, the cost of

the sensor must be offset by the reduction in the cost of the other elements of the process or by the enhancement in the yield.

The control system development procedure used in the process synthesis program is depicted in Figure 16. The first step is concerned with model development using a finite element procedure. This model is then perturbed in a specific predetermined manner to obtain information that can be used to develop a dynamic control model. Control design and analysis tools are then used to design a controller. These analysis tools are used to evaluate the intrinsic and extrinsic behavior of the controller. The controller is then evaluated in closed-loop using the finite element simulator.

One particular application for the development of a multivariable, wafer temperature controller for RTP is shown in Figure 17. After exciting the inputs to the finite element model, the data was fit to a high-order linear set of ordinary differential equations (ODEs) relating the input lamp power to the output wafer temperature. This high order set of ODEs was reduced to remove the unimportant states. The reduced order model was then used in the design of a Kalman filter to estimate the model states. The estimated states were then integrated into the design of a linear quadratic regulator. The controller was then evaluated using the high-order set of ODEs as the actually system. If the response was poor, the controller was redesigned. Otherwise, the controller was evaluated using the nonlinear finite element simulator. If the results were not to specification, the control design procedure was reevaluated. If the results were acceptable, the controller was then implemented and tested in hardware. By developing the control design in a virtual environment, substantial benefits can be realized since the simulator can be used instead of the actual equipment. This results in a time and materials savings.

This methodology of controller development was conducted in conjunction with Sandia National Laboratories (Livermore, CA) who had developed a detailed nonlinear finite element simulator of an RTP system. The controller developed in SIMULINK is graphically depicted in Figure 18. This graphical depiction is actually "active". Each block can be opened by clicking on it with the mouse. The block can be used to specify the design parameters of the controller. Fast numerical simulation was enacted so that the controller can be quickly evaluated. The process block was comprised of a state-space description of the high-order set of ODE's obtained by analyzing system excitation data from Sandia's finite element simulator.

After the controller satisfactorily achieved the objectives using the linear simulation models, it was formulated for testing using the Sandia finite element simulator. Some results are shown in Figure 19. The figure illustrates the temperature response of a silicon wafer to a controlled ramp from 800 to 1100°C at 40°C per second. The lamp powers required to provide the controlled ramp are also shown. The spatial temperature nonuniformity was the key parameter to evaluate the performance of the controller. It was seen that good control was obtained. In addition, it was possible to evaluate the nonuniformity over the entire wafer. This was a valuable computation which was only possible through the use of a detailed simulator.

One of the benefits of a concurrent engineering, process synthesis approach was that one could analyze performance characteristics by asking "what if" questions. This is demonstrated in the plots of Figure 20. This evaluation was conducted by designing the controller for operation on a blank wafer. Then the controller was evaluated for the case where patterning was present inducing changes in the emissivity and radiant heat transfer characteristics. This case was representative of how the controller would behave in an actual processing situation. It was shown by the simulator that the controlled power oscillated but otherwise maintained good temperature control at the sensor locations. There was intersensor rippling of the temperature however. This effect can not be compensated by the controller design but must taken into account during the reactor design phase.

3.3 Intelligent Design of Experiments and Recipe Synthesis

One of the main taks in designing equipment CAD and virtual reactor is intelligently consolidating the model and experimental data. Through an efficient design of experiments and optimization it is possible to

not only fit the data to the model but also synthesize the optimal operating points. Figure 21 illustrates a method of combining model and experimental data to obtain an improved simulator with minimized error. The improved simulator is based on combining the physics-based model with a correction function which accounts for the deviation of experimental results from the original model. The figure illustrates the simulation of the oxide thickness as a function of variation in wafer temperature and process time around the optimal setting of T=1007.4°C and t=185.7sec.

Figure 22 illustrates a 24 wafer oxidation run incorporating both wafer to wafer as well as within wafer thickness variations. Recipes can be obtained by varying and iterating the setpoints of the virtual reactor to minimize the variations. The optimized setpoints (temperature, time, pressure, etc.) can be used as the starting point for actual wafer processing.

Figure 23 illustrates a five wafer simulated run of a gate stack consisting of polysilicon on oxide. As with the wafer oxidation run, wafer to wafer and within wafer variations are simulated. By iterating on the process parameters for both the oxide growth and polysilicon RTCVD, an optimum recipe for the gate stack can be obtained.

4 Conclusion

Our work addressed the development and demonstration of a framework for a virtual reactor that includes equipment CAD, recipe synthesis, and sensing/control capabilities. In our approach, the virtual reactor was represented in a detailed computational architecture to achieve improved understanding of the critical underlying processing parameters with respect to:

- Equipment design and improvement.
- Optimum recipe generation with minimum iterations and experimental data.
- Virtual process, sensor fusion and control runs.

In developing our approach to analyze and design semiconductor manufacturing technology from a process synthesis/virtual reactor perspective, a strong foundation was established to pursue follow-on research and development activities. Our objective was to systematize equipment and process development via models, to reduce the iterations in the designs of novel sensors, and to achieve rapid equipment and unit process development. Advancements in these areas will reduce non-recurring engineering cost and reduce the time required to produce a robust IC fabrication equipment and unit processes. These advancements not only improve the economic viability of low and high volume private semiconductor corporations but also enhance the capability to quickly manufacture integrated circuits for military applications.

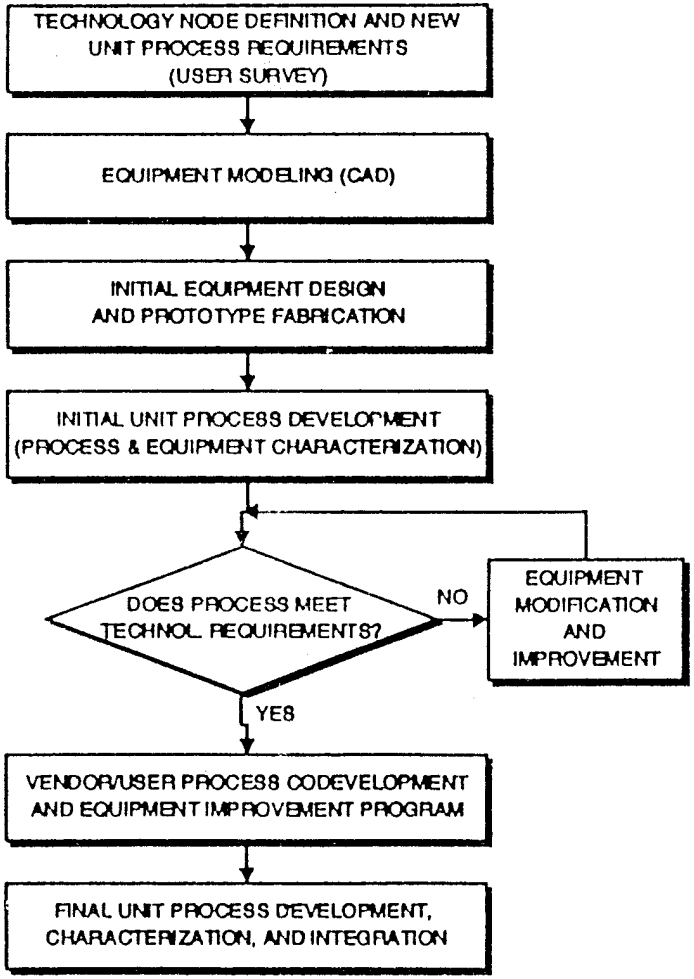

Fig. 1: Current state-of-the-art methodology for equipment design.

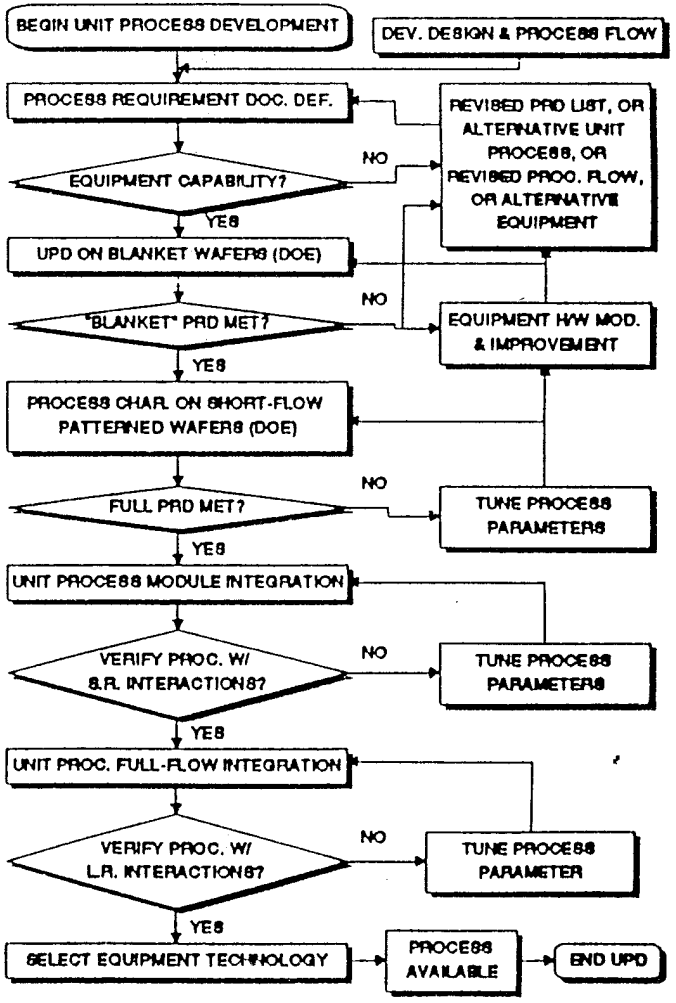

Fig. 2: Current state-of-the-art methodology for development, characterization, and integration of unit processes.

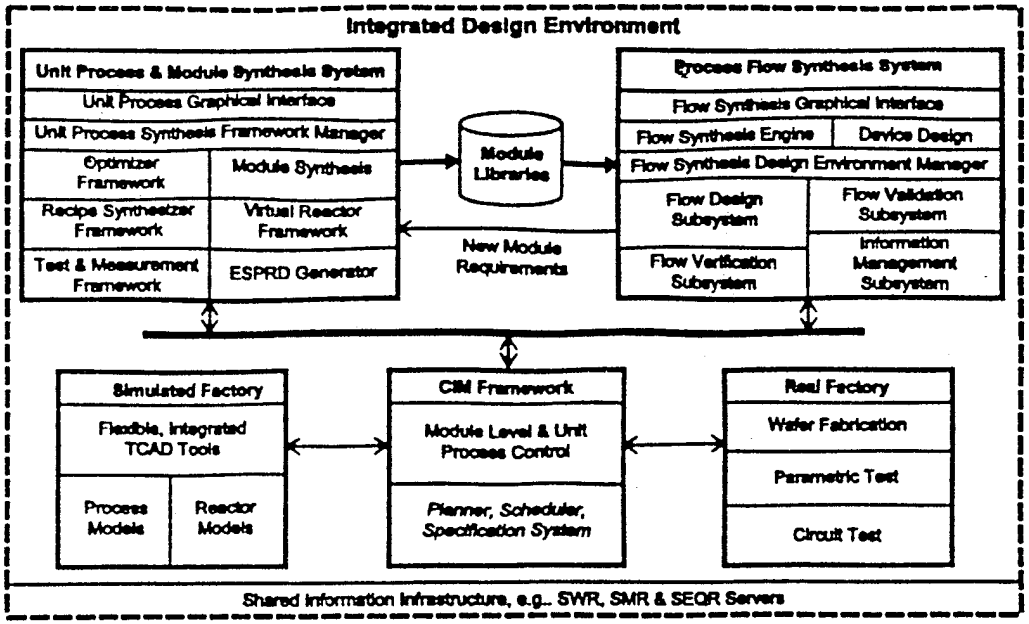

Fig. 3: Systematic flow synthesis architecture.

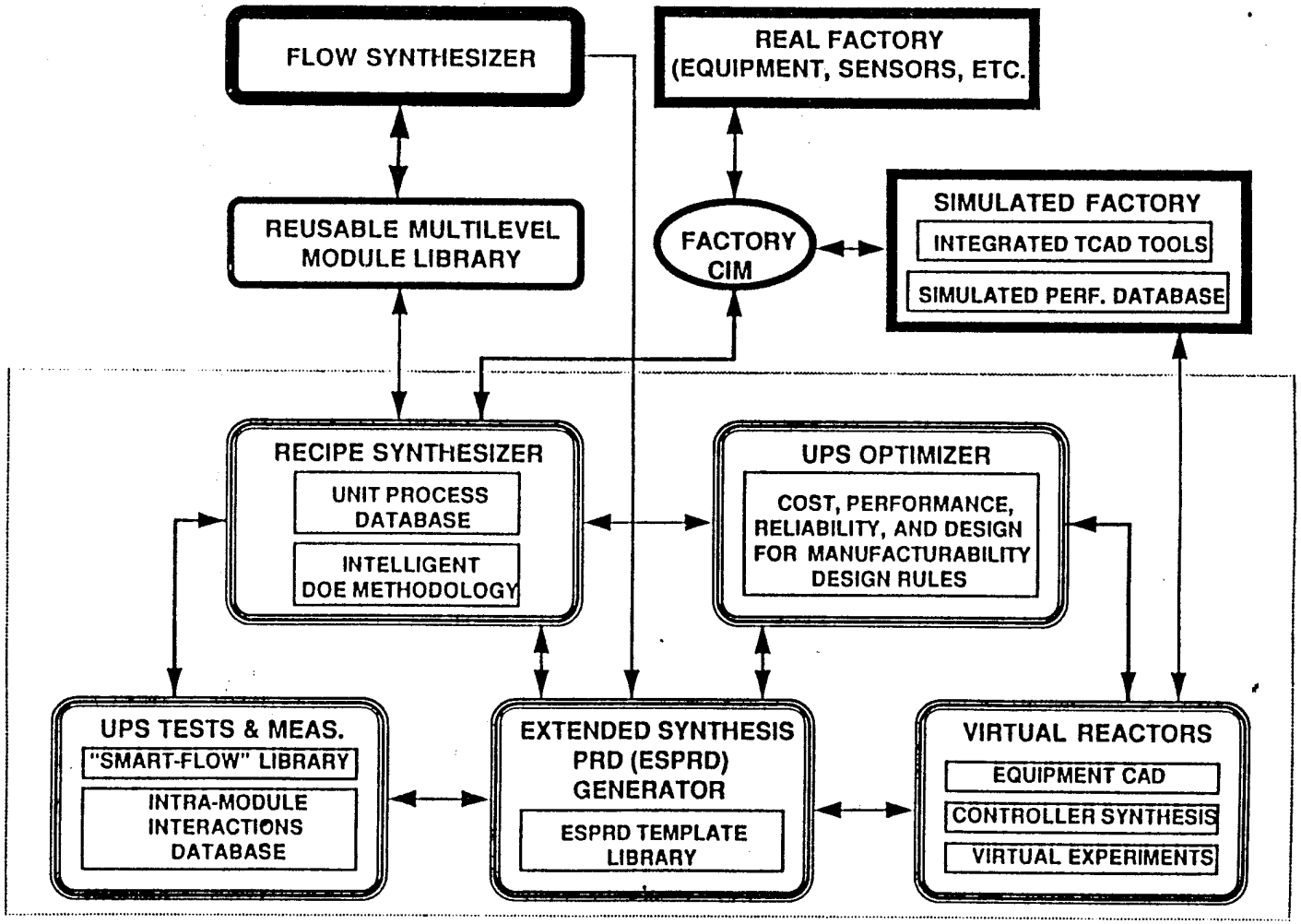

Fig. 4: Overall unit process and module synthesis environment.

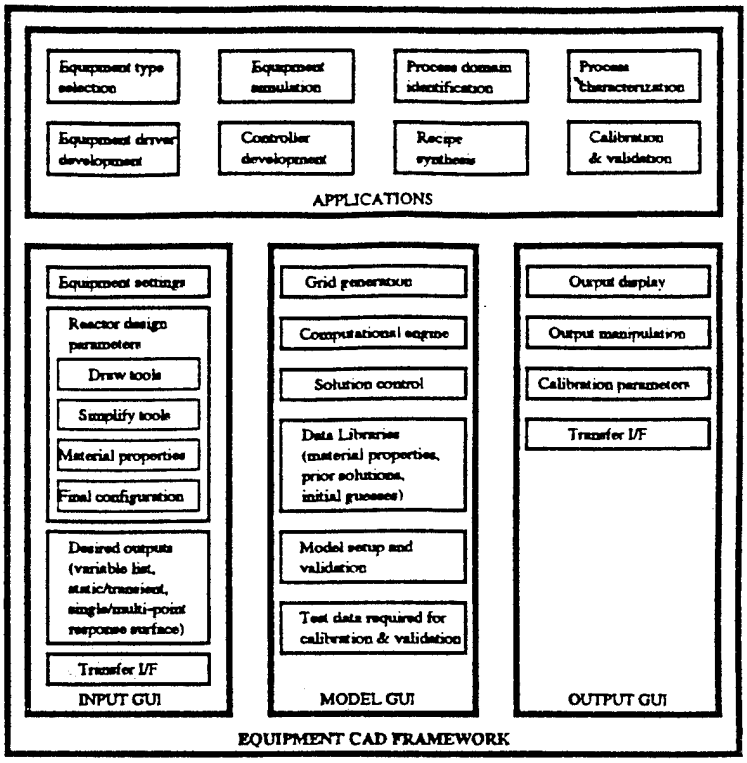

Fig. 5: Suggested equipment CAD framework for process synthesis.

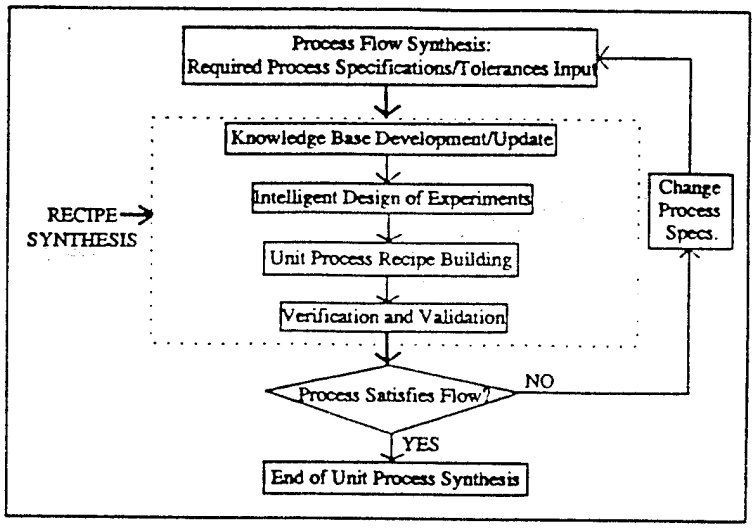

Fig. 6: Recipe synthesis within unit process synthesis.

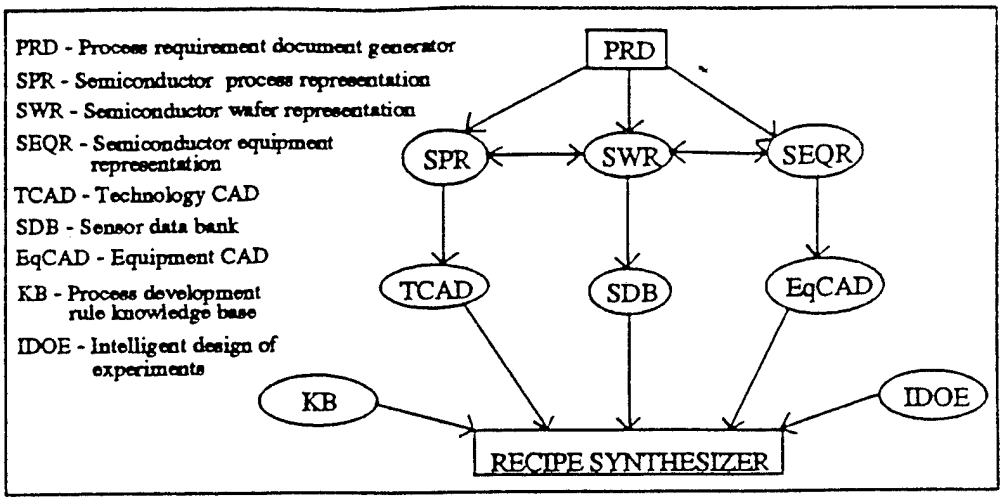

Fig. 7: Recipe synthesis framework.

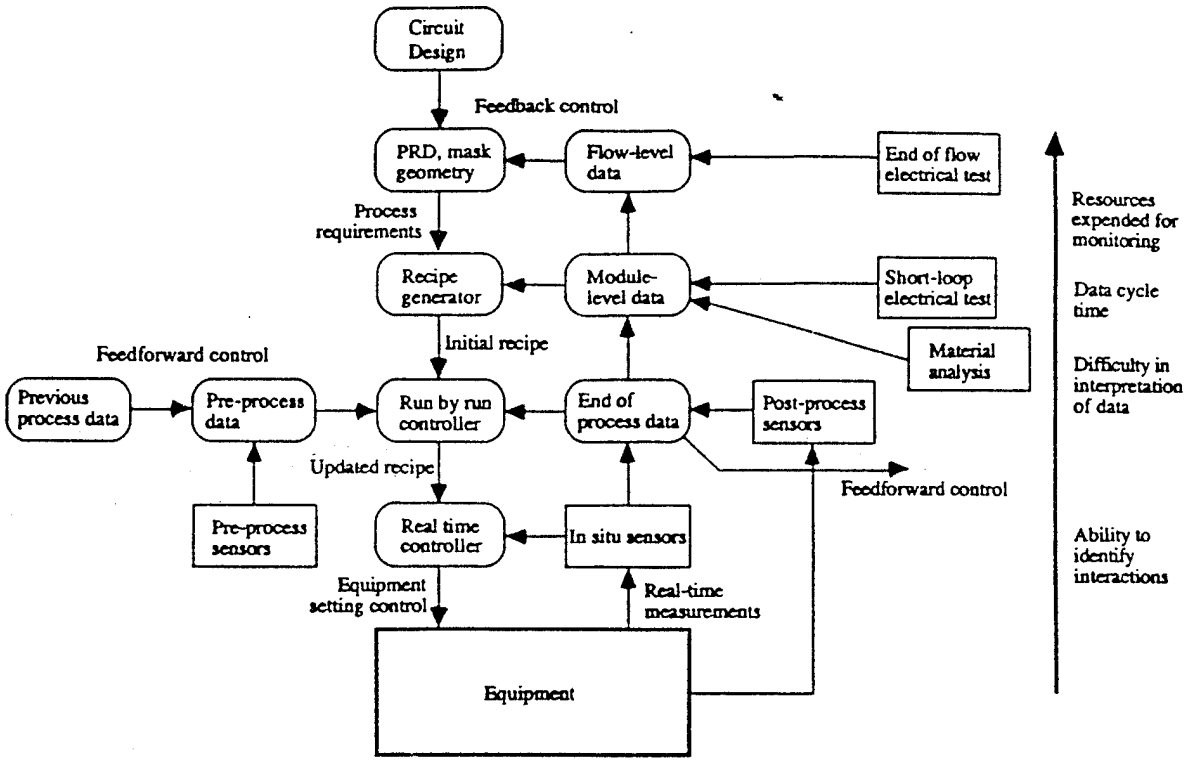

Fig. 8: Levels of hierarchy in process control.

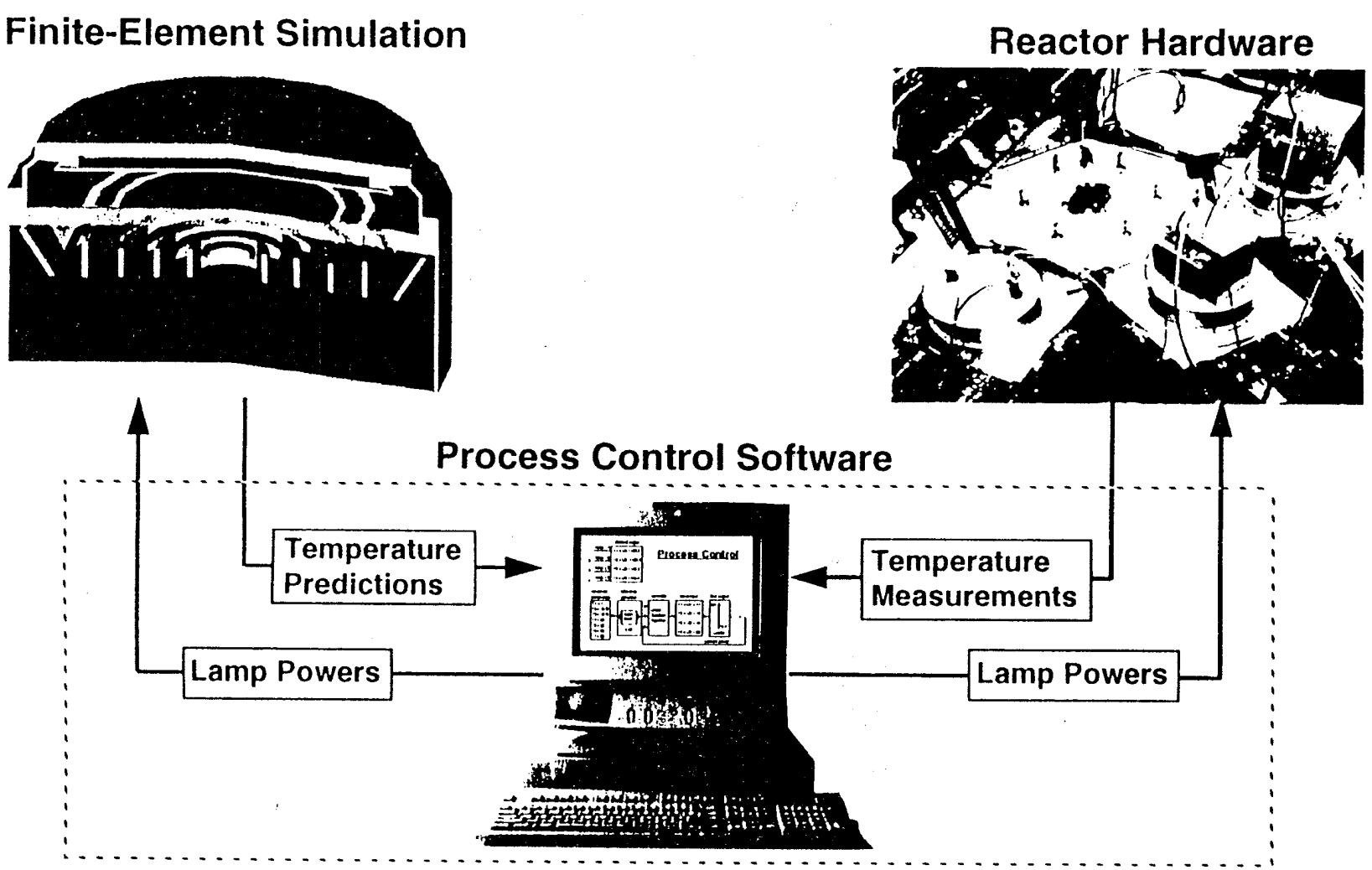

Fig. 9: Linking process control software, finite-elment simulators, and reactor hardware.

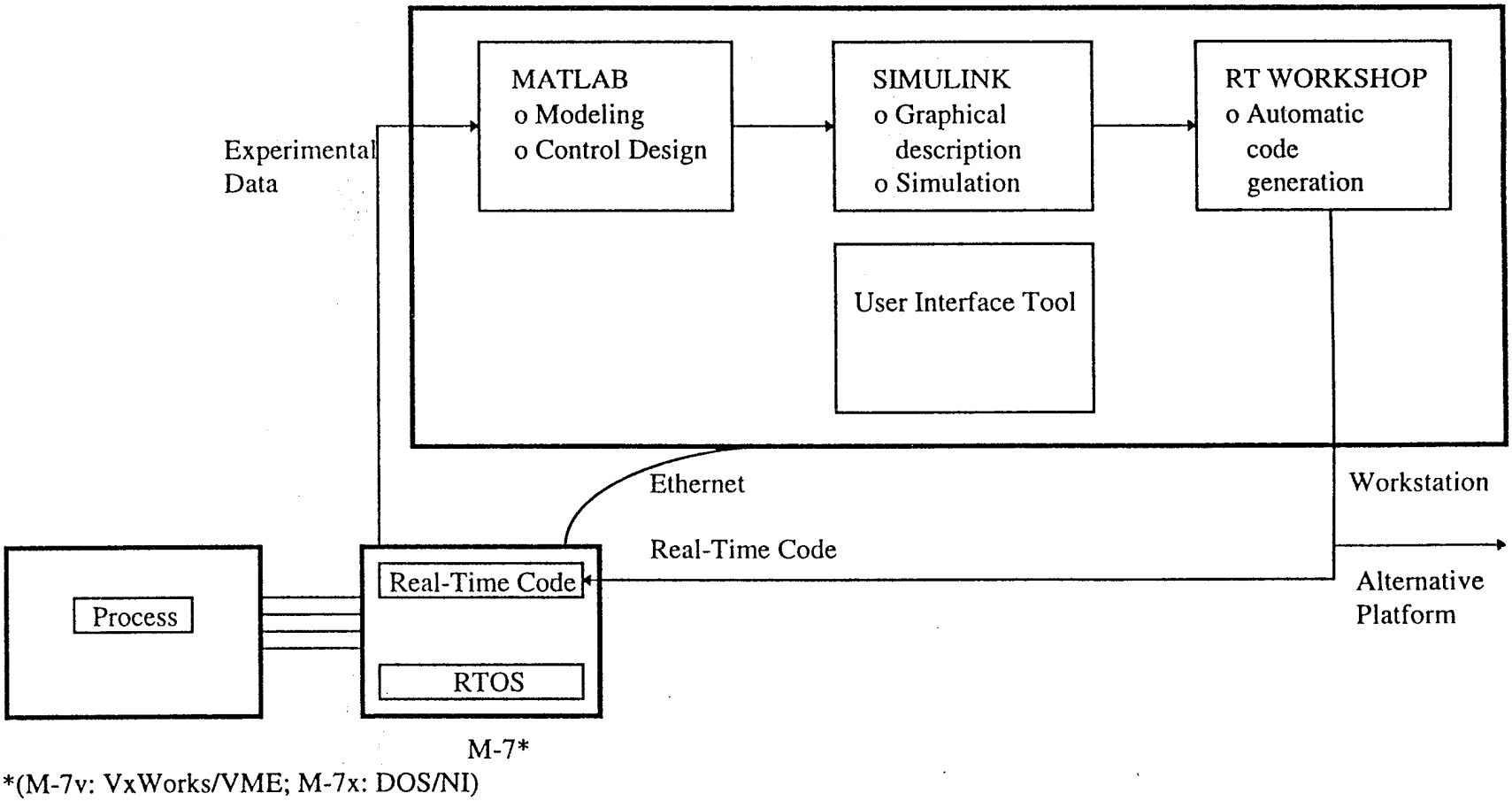

Fig. 10: Process synthesis control development environment.

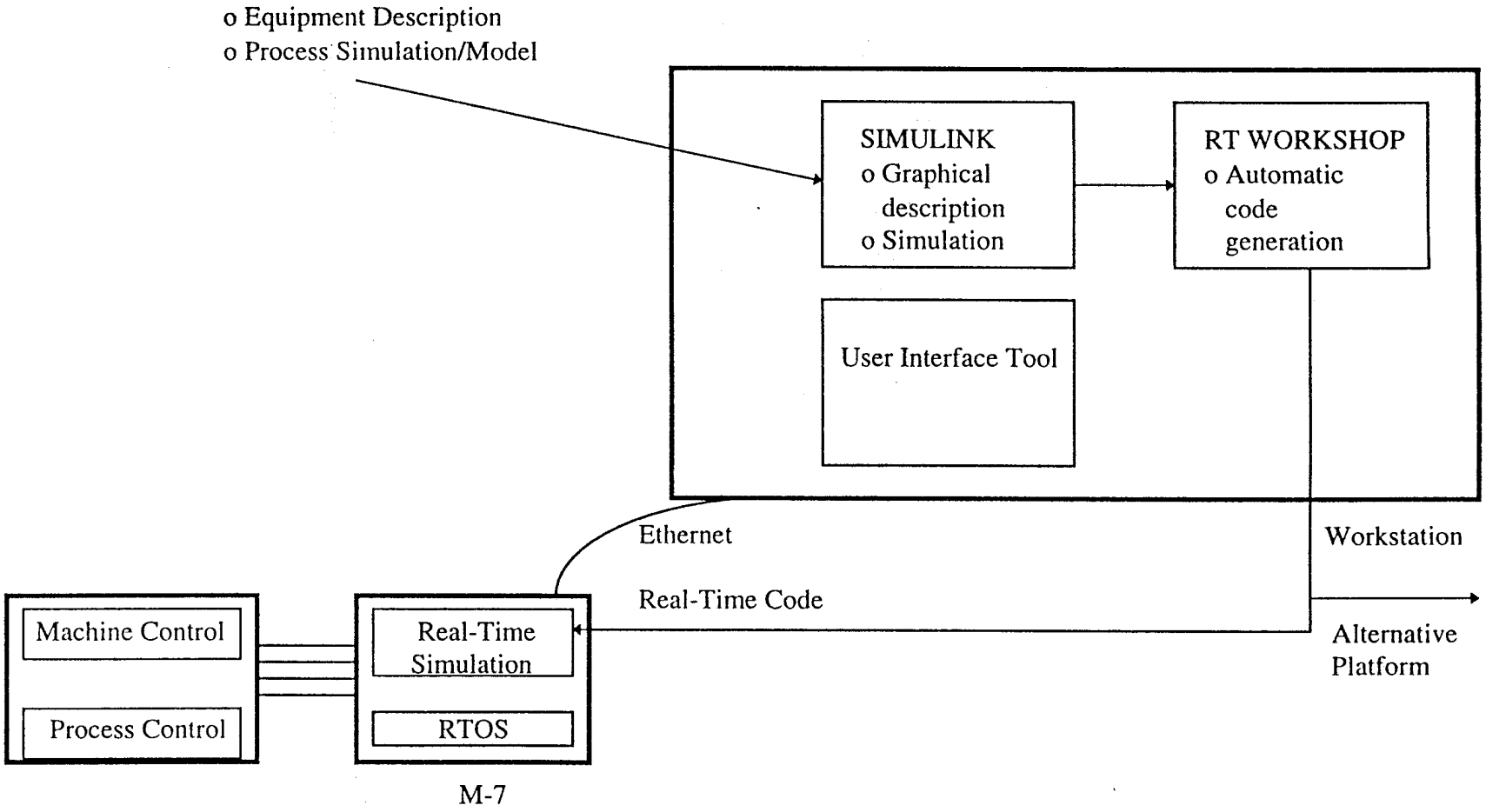

Fig. 11: Process synthesis simulation development and implementation environment.

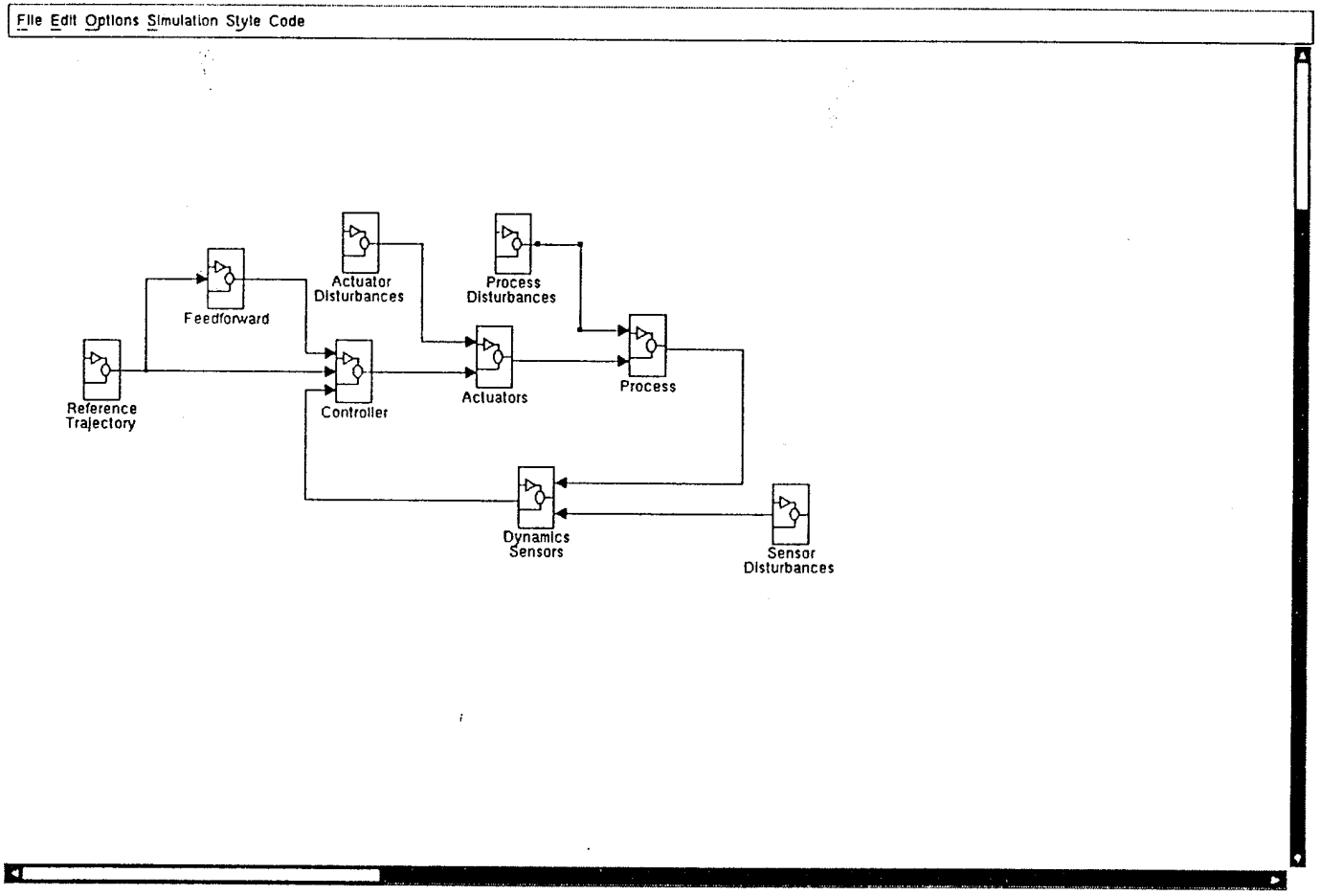

Fig. 12: Modeling architecture to simulate closed-loop control of wafer temperature as well as the real-time growth of oxide and polysilicon films.

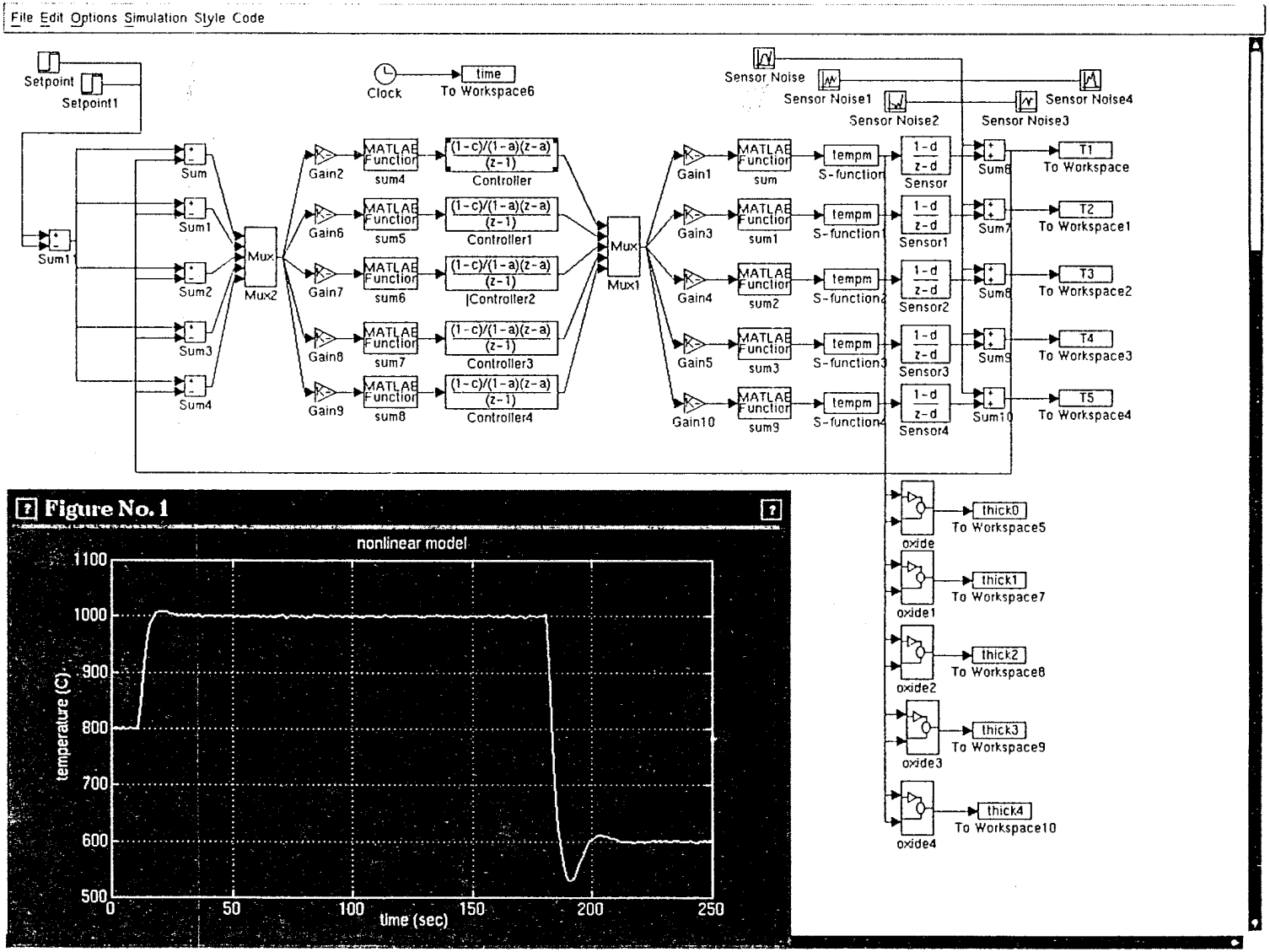

Fig. 13: Simulation of the wafer temperature during a controlled RTP thermal cycle.

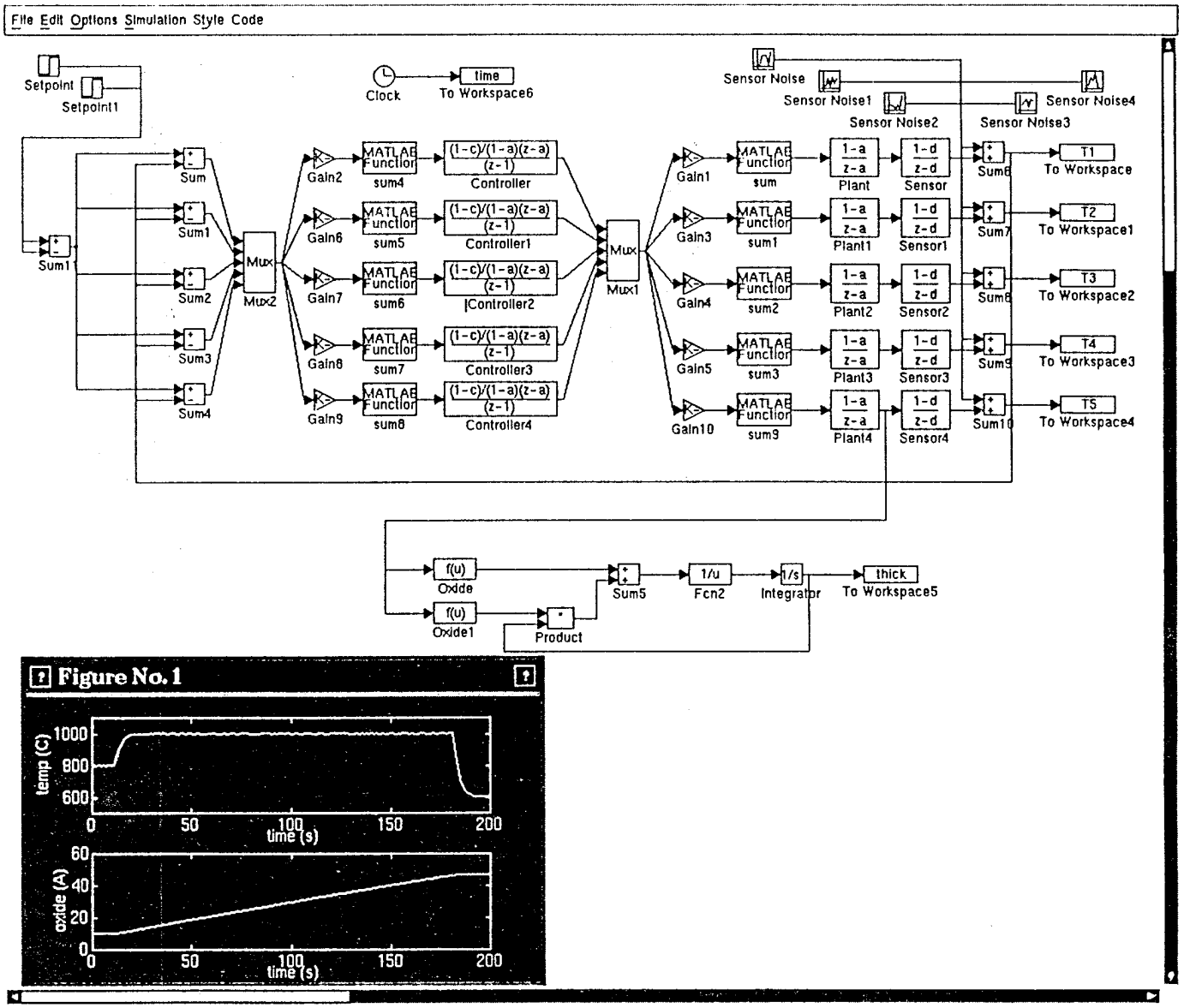

Fig. 14: Simulation of oxide growth.

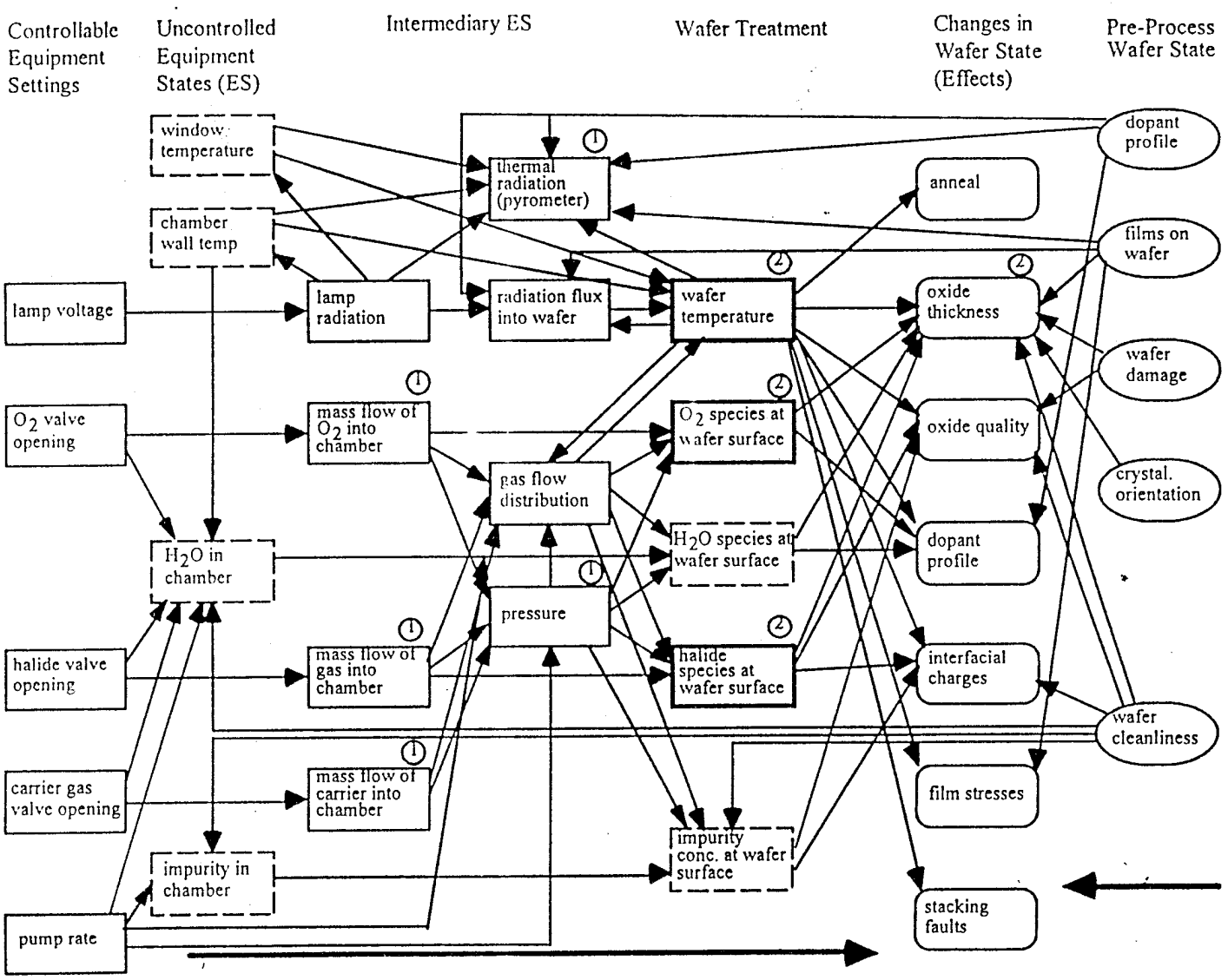

Fig. 15: Optimal sensor set for RTO.

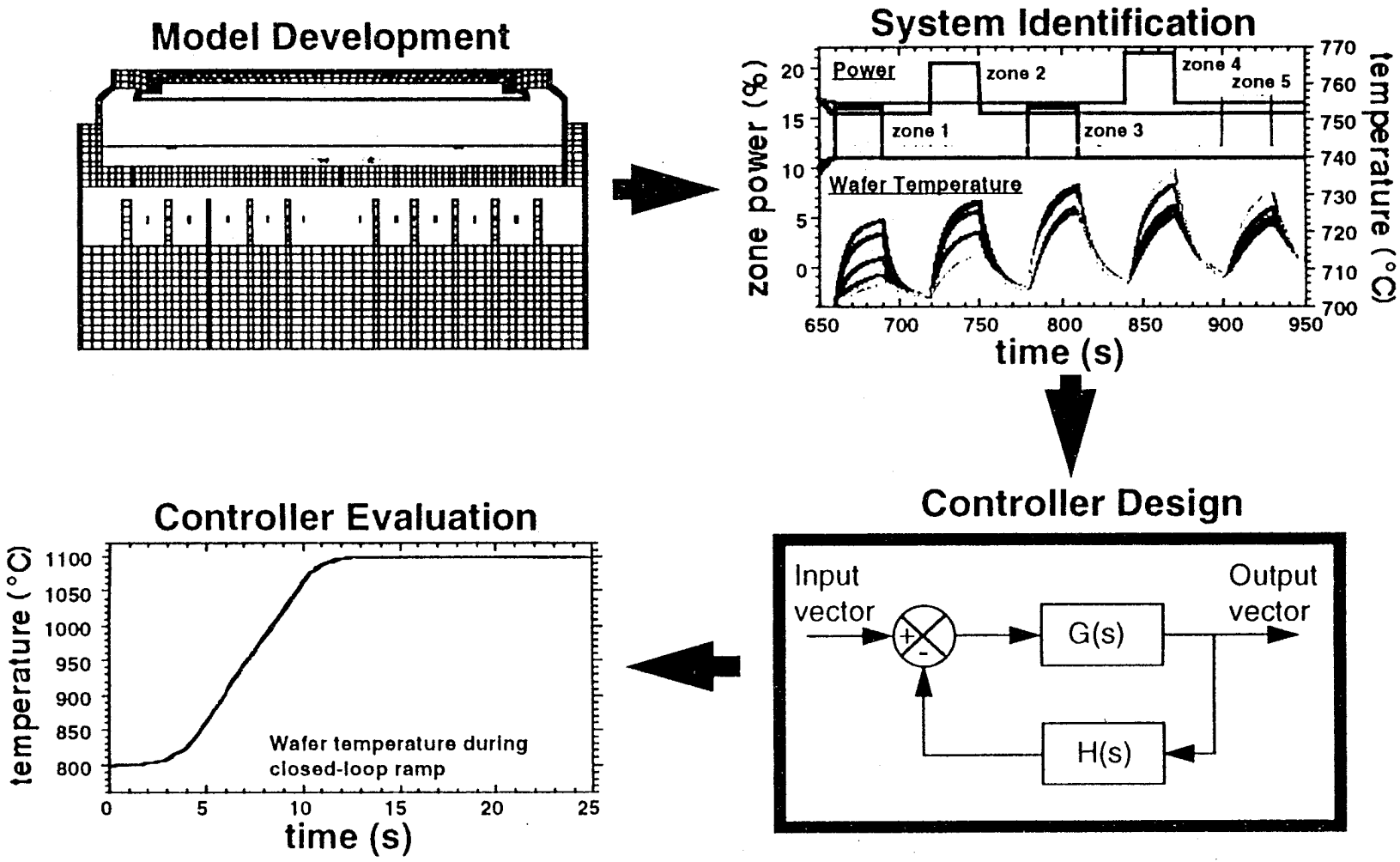

Fig. 16: Control system development procedure employing finite element simulation.

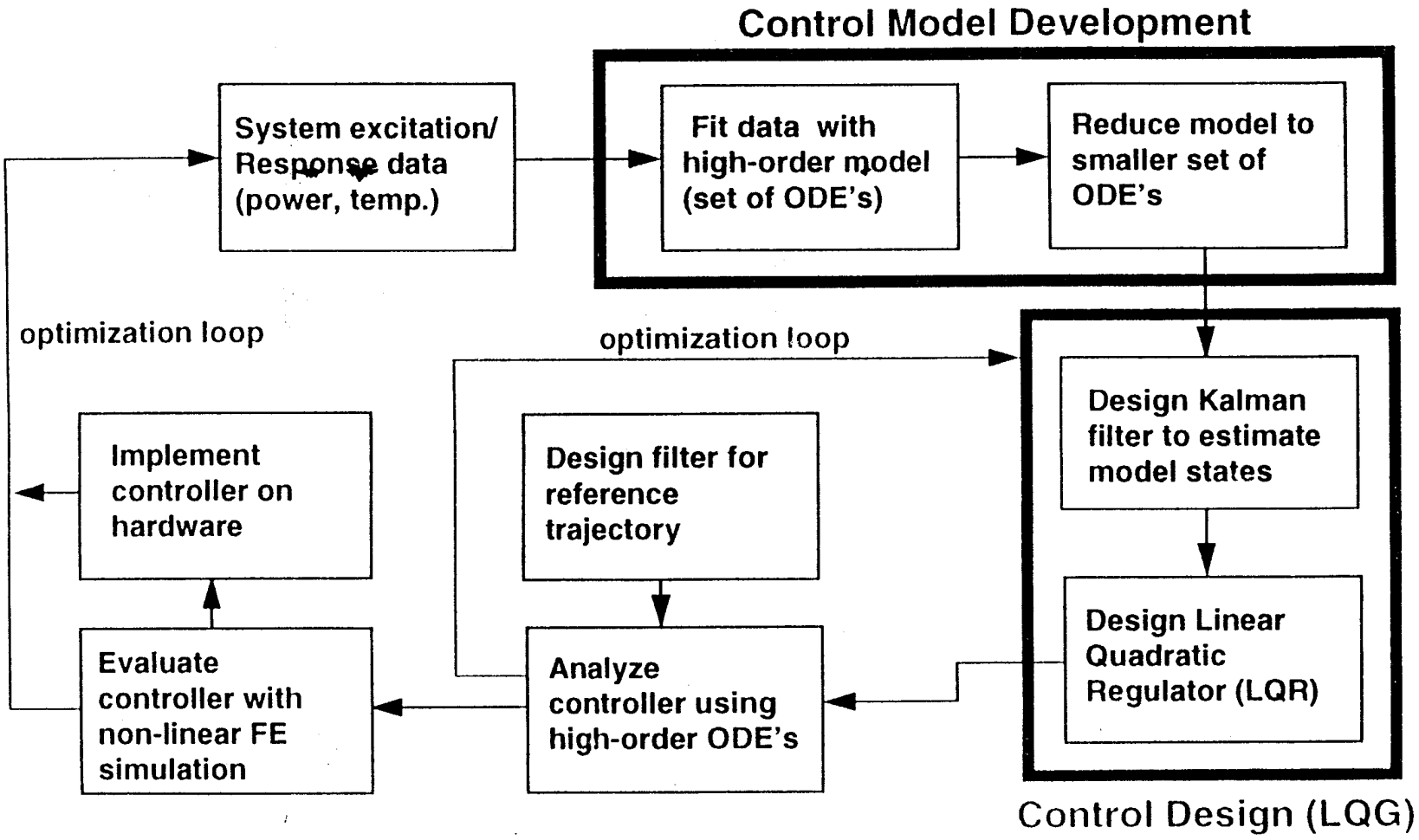

Fig. 17: Approach used to develop a multivariable, wafer temperature controller for RTP.

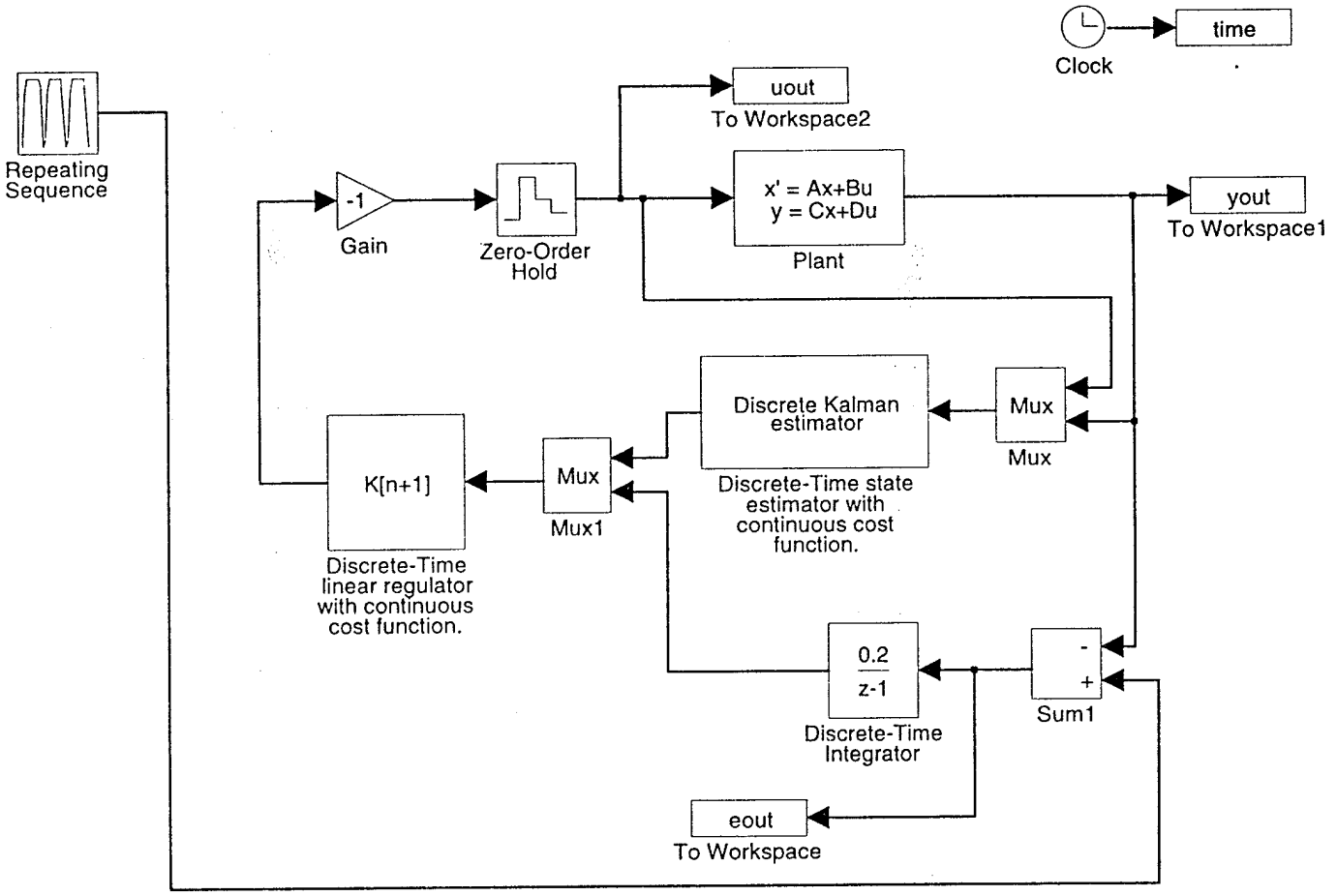

Fig. 18: RTP temperature control development in SIMULINK.

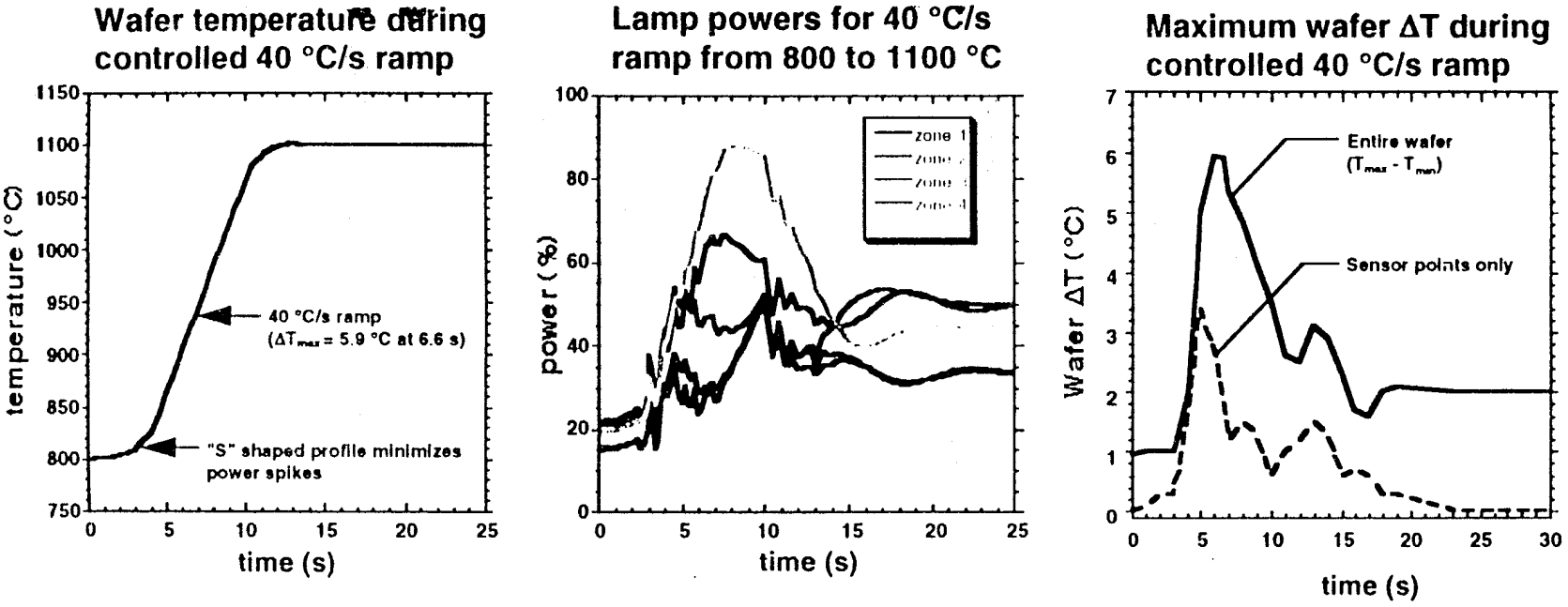

Fig. 19: Results showing temperature controller with Sandia simulator.

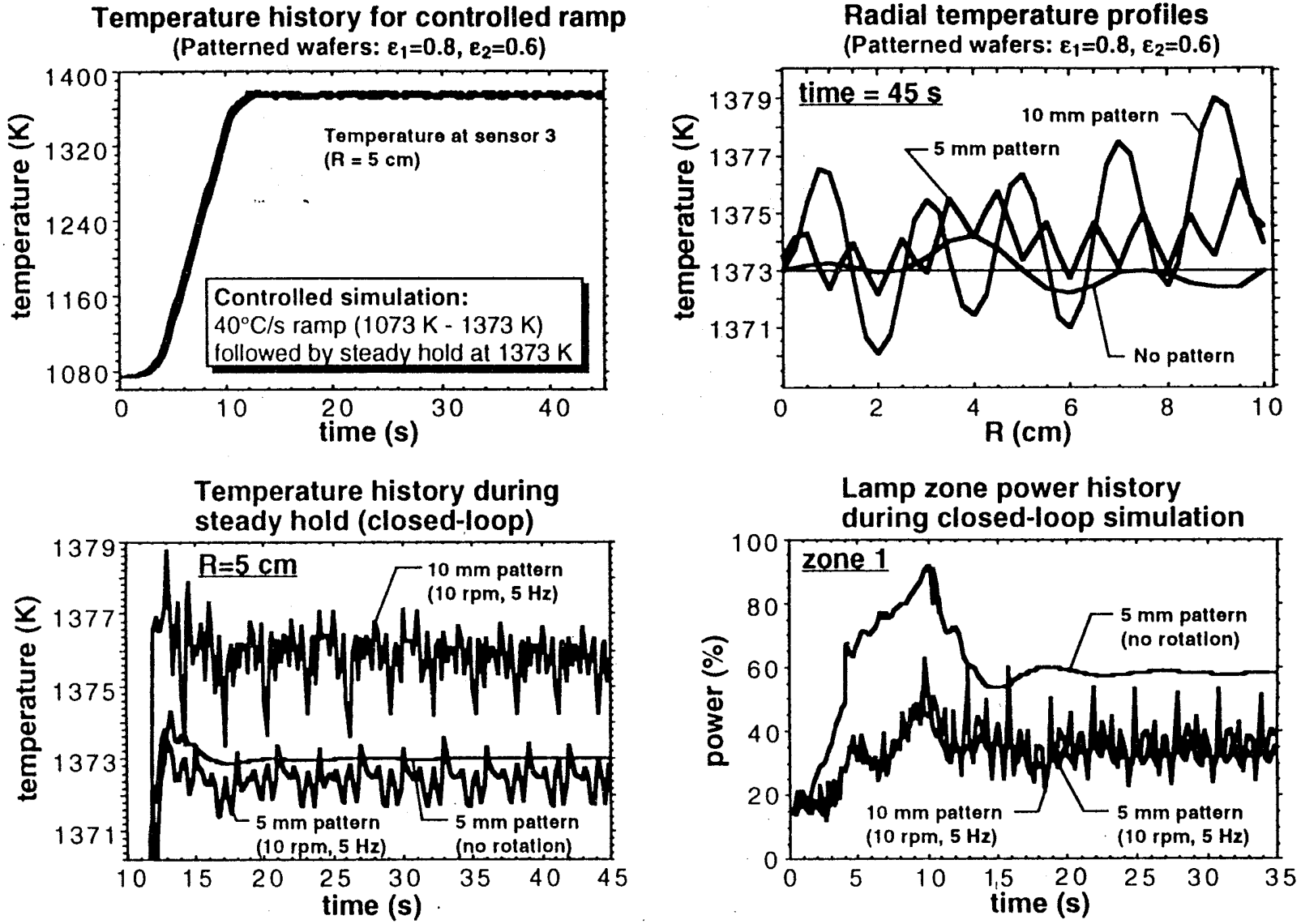

Fig. 20: Analysis of temperature controller with patterned wafer.

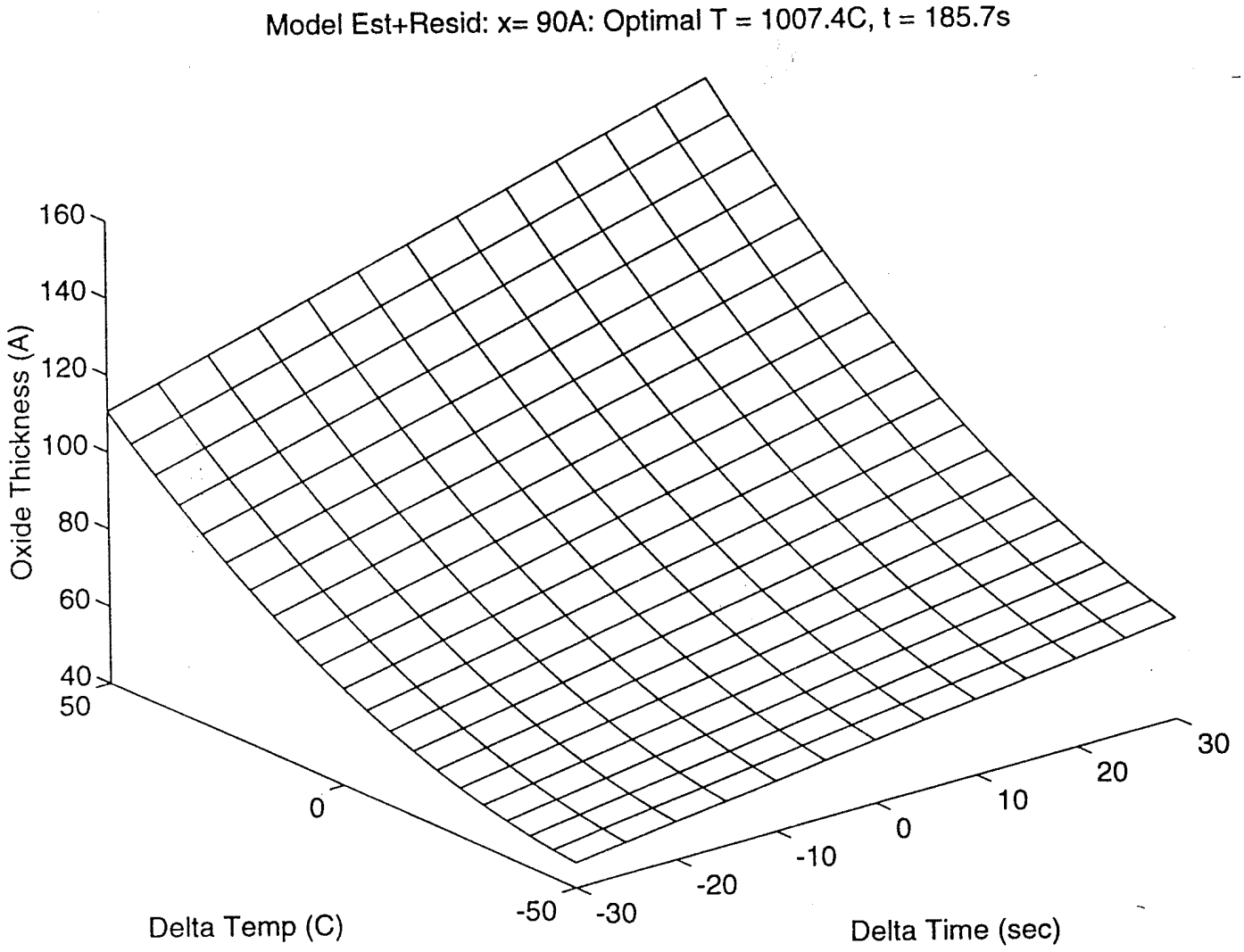

Fig. 21: Combination of model and experimental data to improve predictive capability.

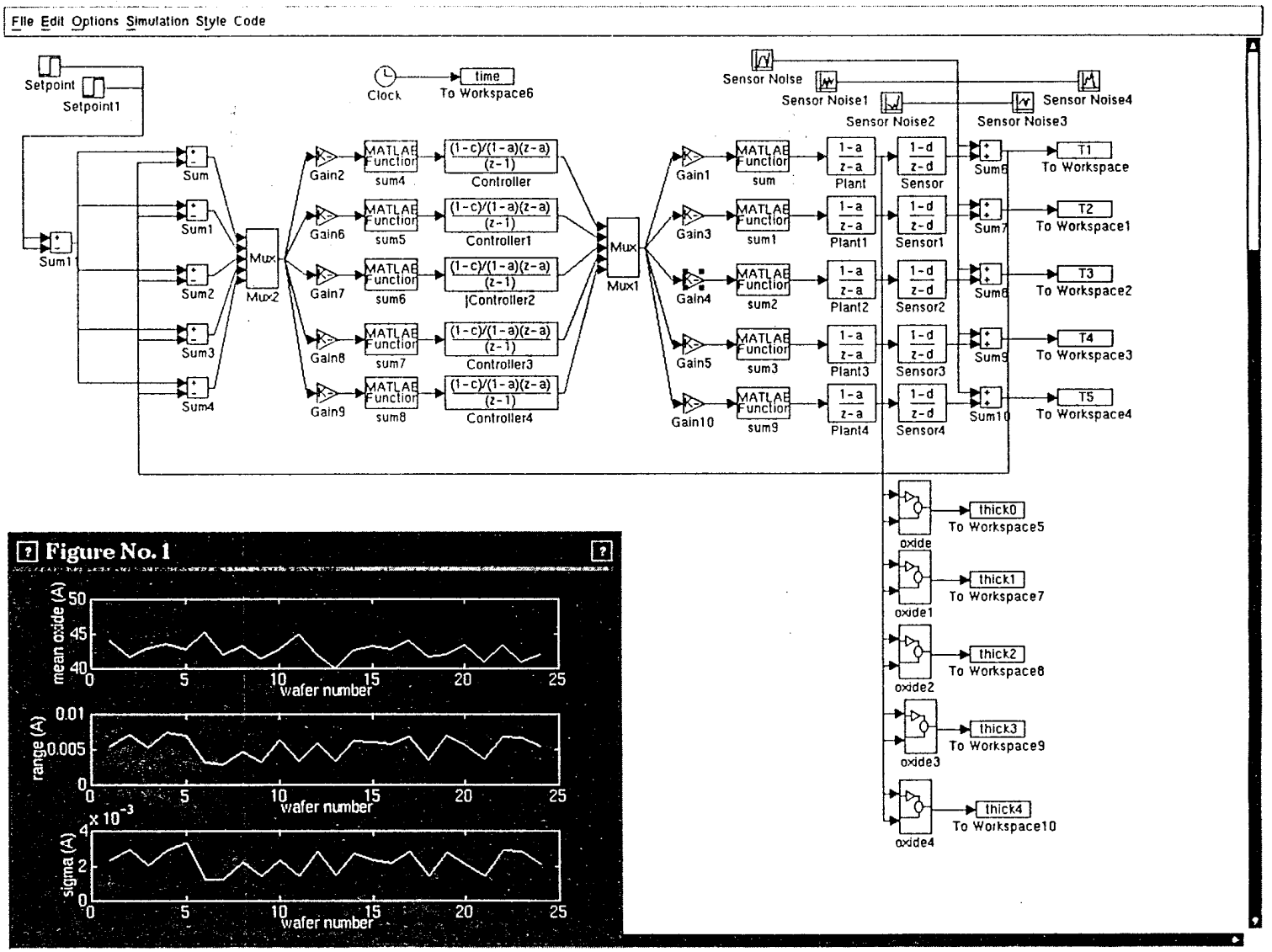

Fig. 22: A 24 wafer oxidation run.

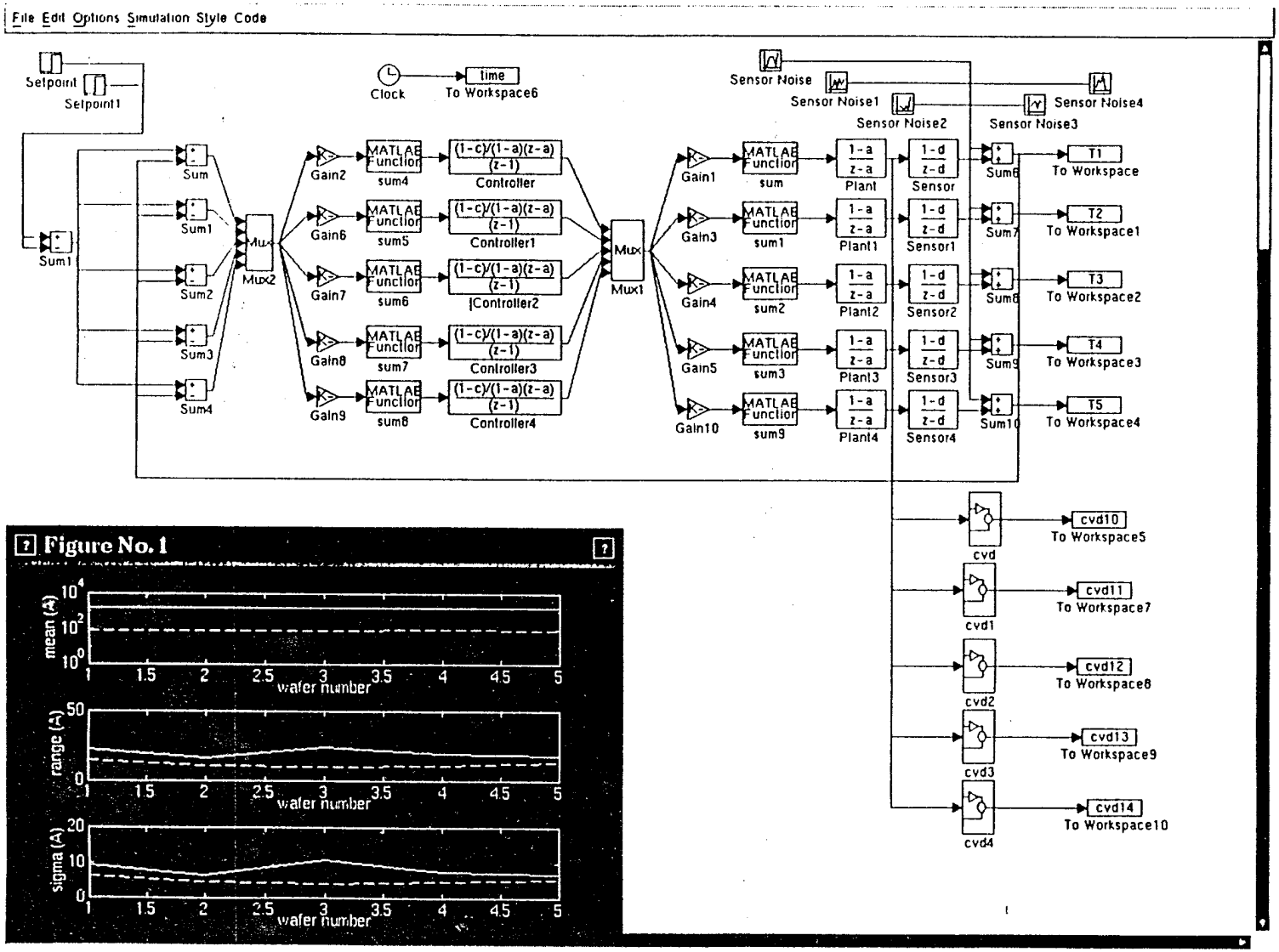

Fig. 23: A five wafer gate stack run of polysilicon on oxide.